A Tale of Two Interfaces

DVB/ASI – SMPTE 310

Andy Butler

Sr. Director – Engineering

Today’s Presentation

- Brief Review of Each Standard
- Strengths and Weaknesses Analyses
- Practical Implementation Tips
- Sources for Additional Information
- Q&A

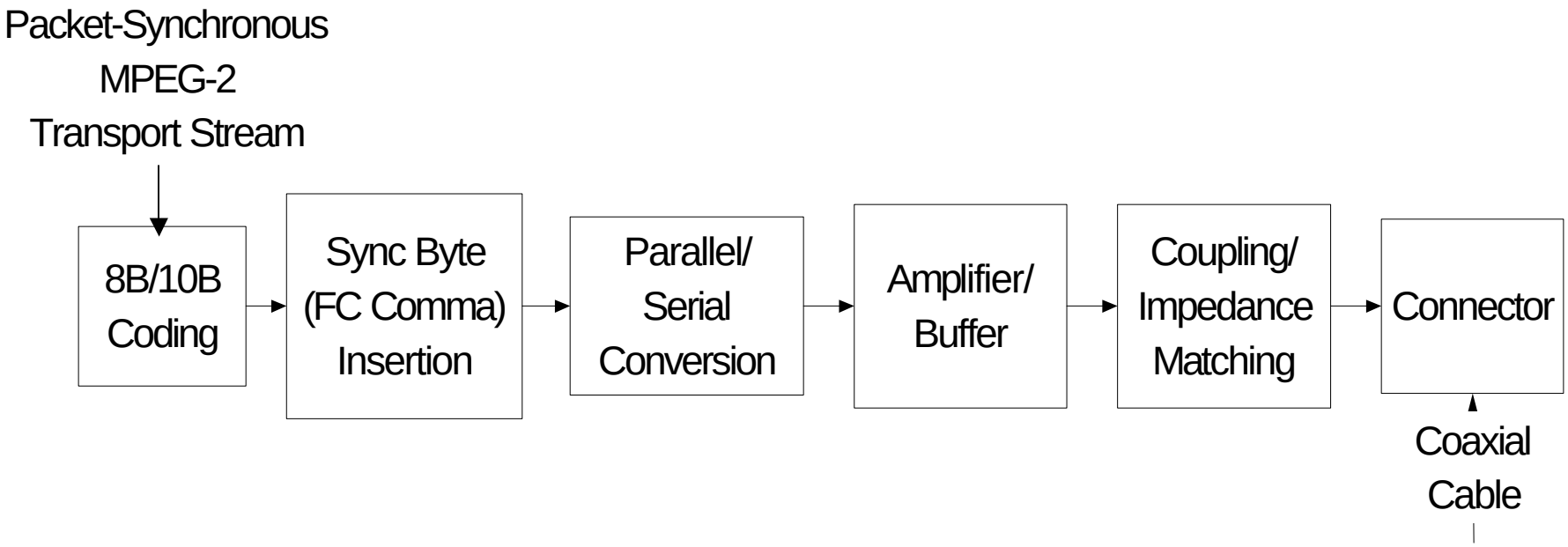
DTV Interface/Transport Summary

- Full Bandwidth 1.5 gbit HD
- Full Bandwidth 270 mbit SD
- Lightly Compressed HD 330 mbit
- Transport Stream – MPEG-2/ATSC
  - SMPTE 310 M
  - ASI/DVB

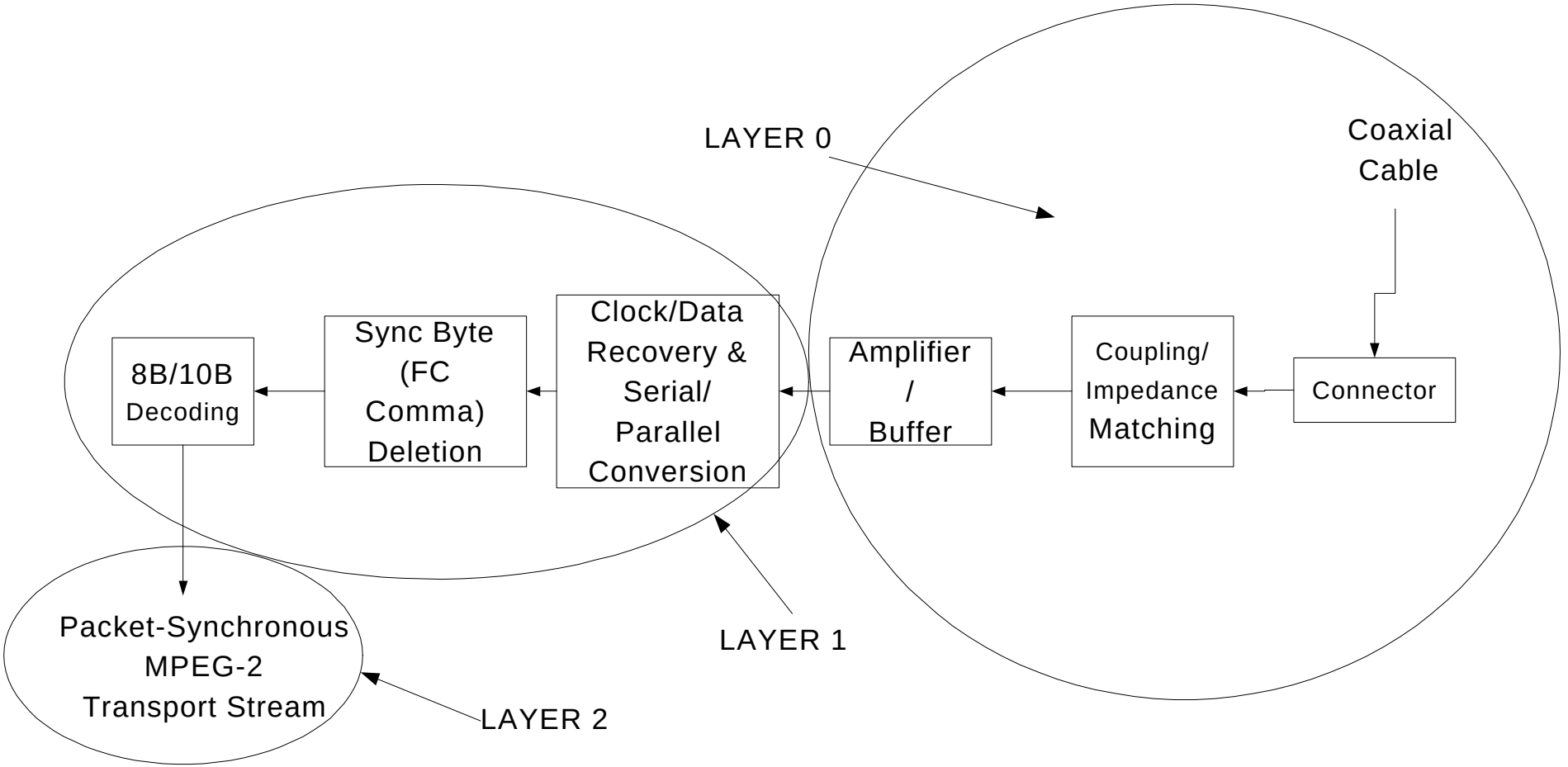
DVB/ASI Family of Standards

- SPI - Synchronous Parallel Interface
- SSI-C - Synchronous Serial Interface on Coaxial Cable
- SSI-O - Synchronous Serial Interface on Optical Fibre
- ASI-C - Asynchronous Serial Interface on Coaxial Cable
- ASI-O - Asynchronous Serial Interface on Optical Fibre

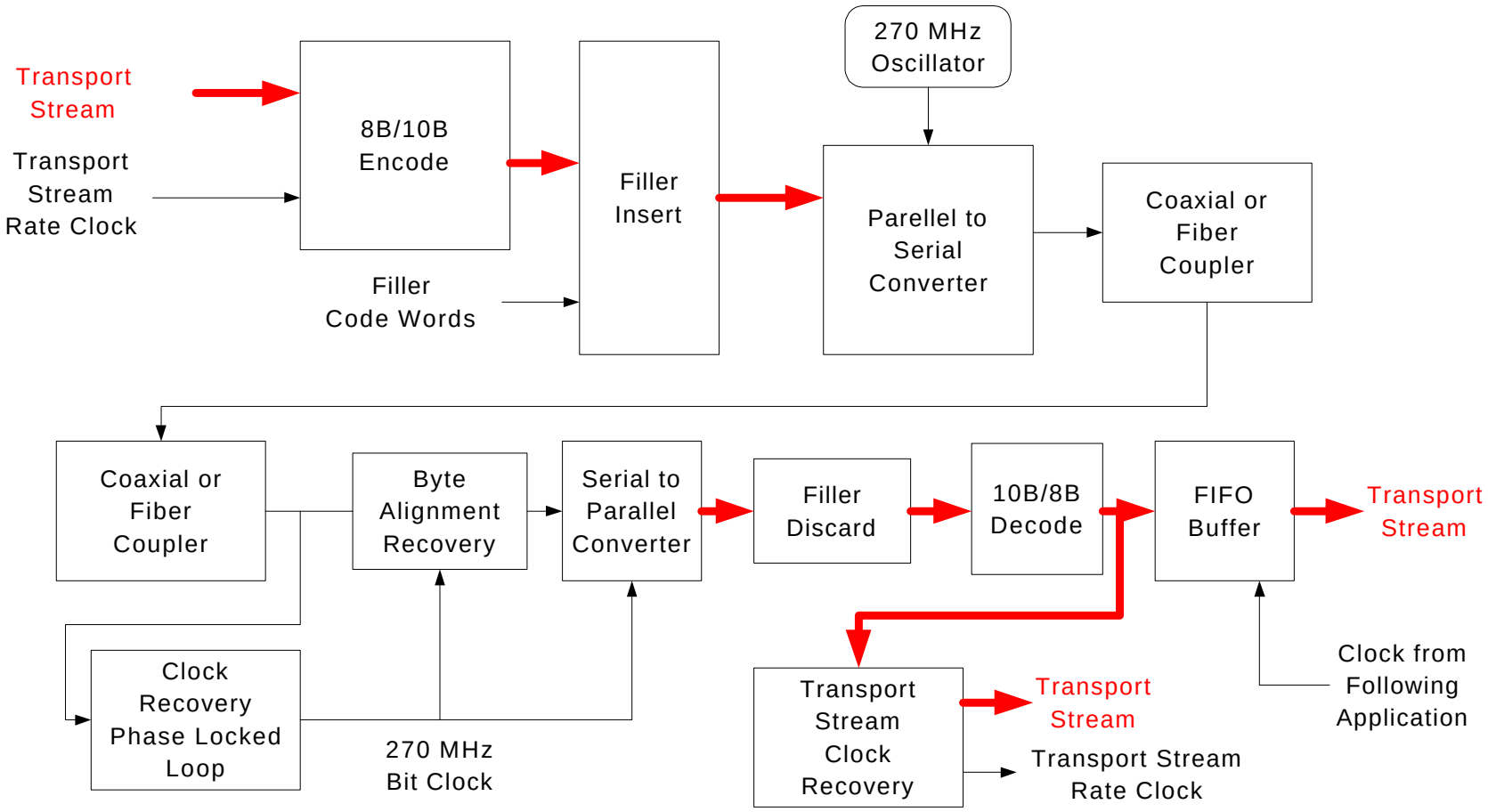
ASI – C - TRANSMIT



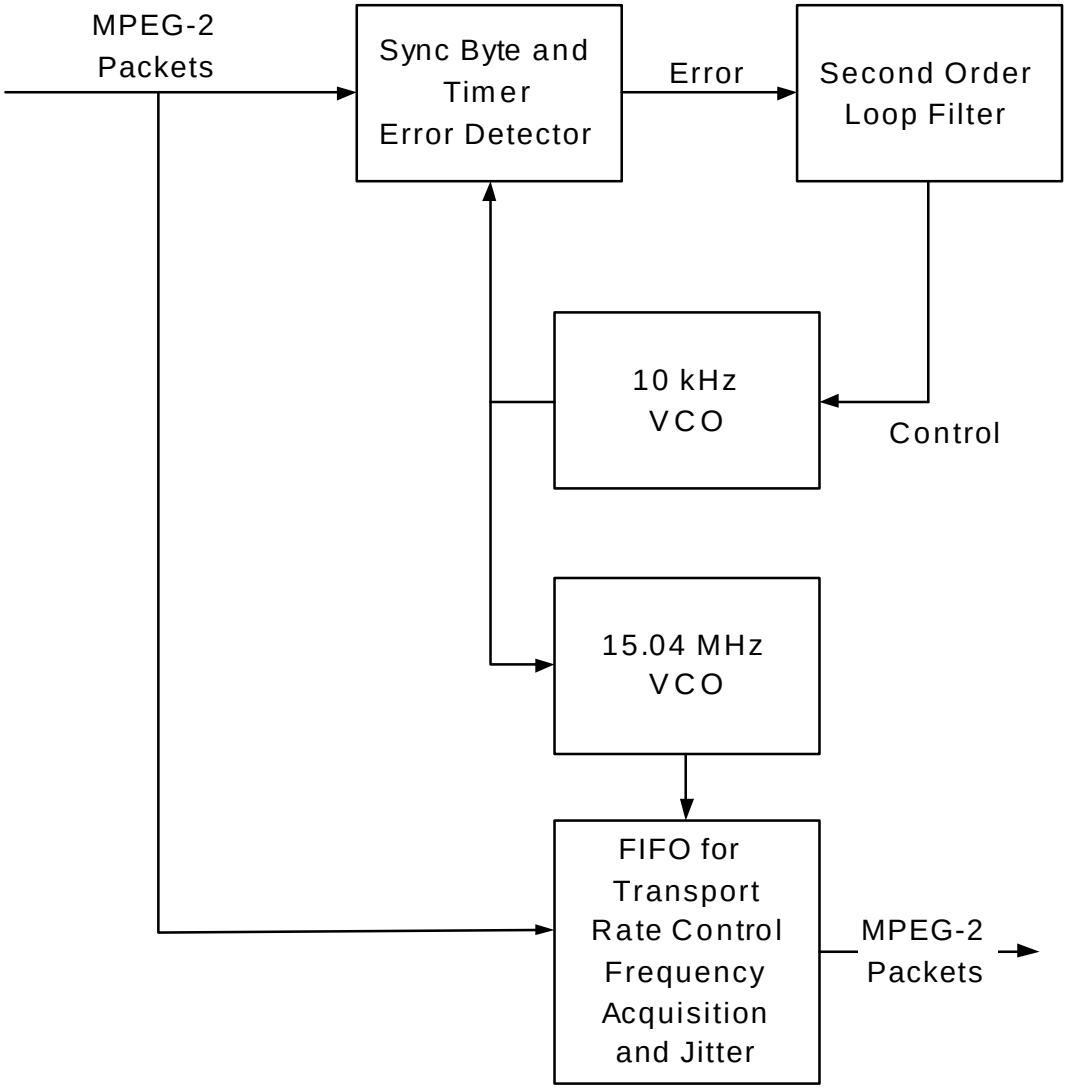
ASI – C - RECEIVE



ASI Clocking Options



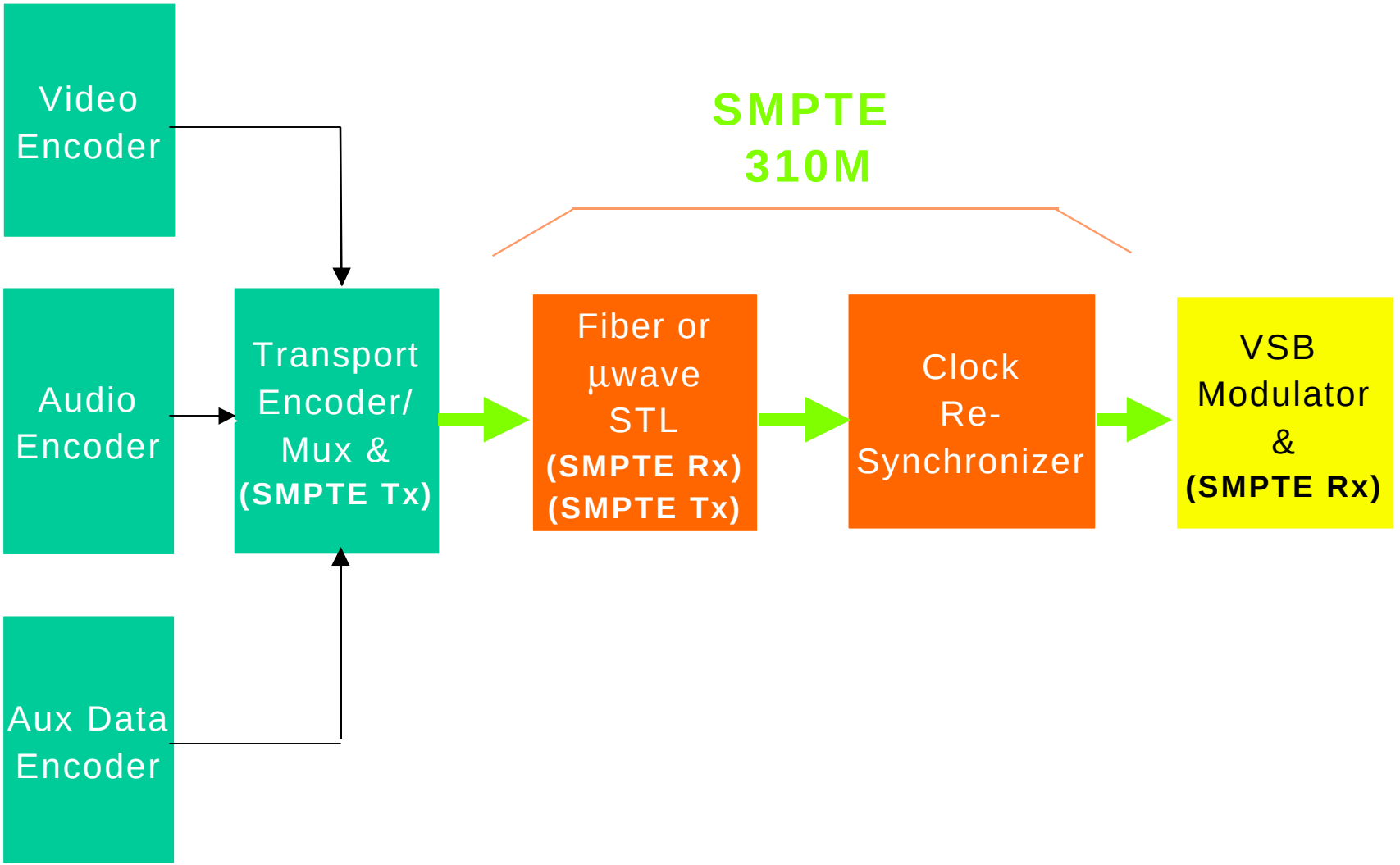
ASI PLL for Clock Generation



Summary of Characteristics

- Fixed Transport Rate – Flexible Payload Rate
- Robust Error Correction
- Deterministic Jitter – 10%
- Random Jitter – 8%
- Output Voltage – 800 mV (p-p)

ATSC Transmitter System Block Diagram



SMPTE 310M DTV Transmitter Interface

Synchronous Serial Interface for MPEG-2 Digital Transport Stream

For 8T-VSB (19.3 Mb/s) and 16-VSB (38.6 Mb/s)

No error correction (for *low noise* environments)

Self-clocking bi-phase mark modulation (MSB first)

Unbalanced 0.8 Vpp centered at 0 Vdc

Single 75 Ω coax with (50 Ω) BNC connectors

Transport clock frequencies:

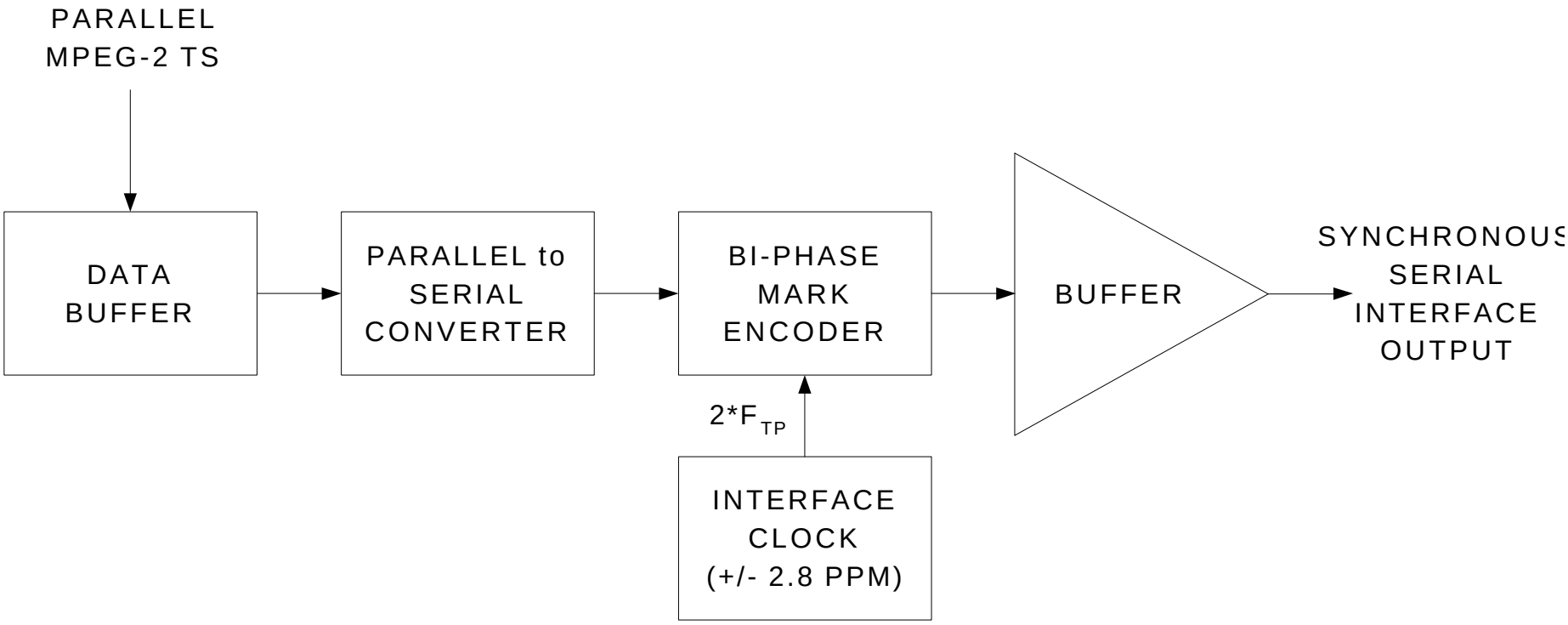
$F_{TRANSPORT} = N * (188/208) * (312/313) * F_{SYMBOL}$

8T-VSB: 19.39265846 Mbits/sec (N = 2)

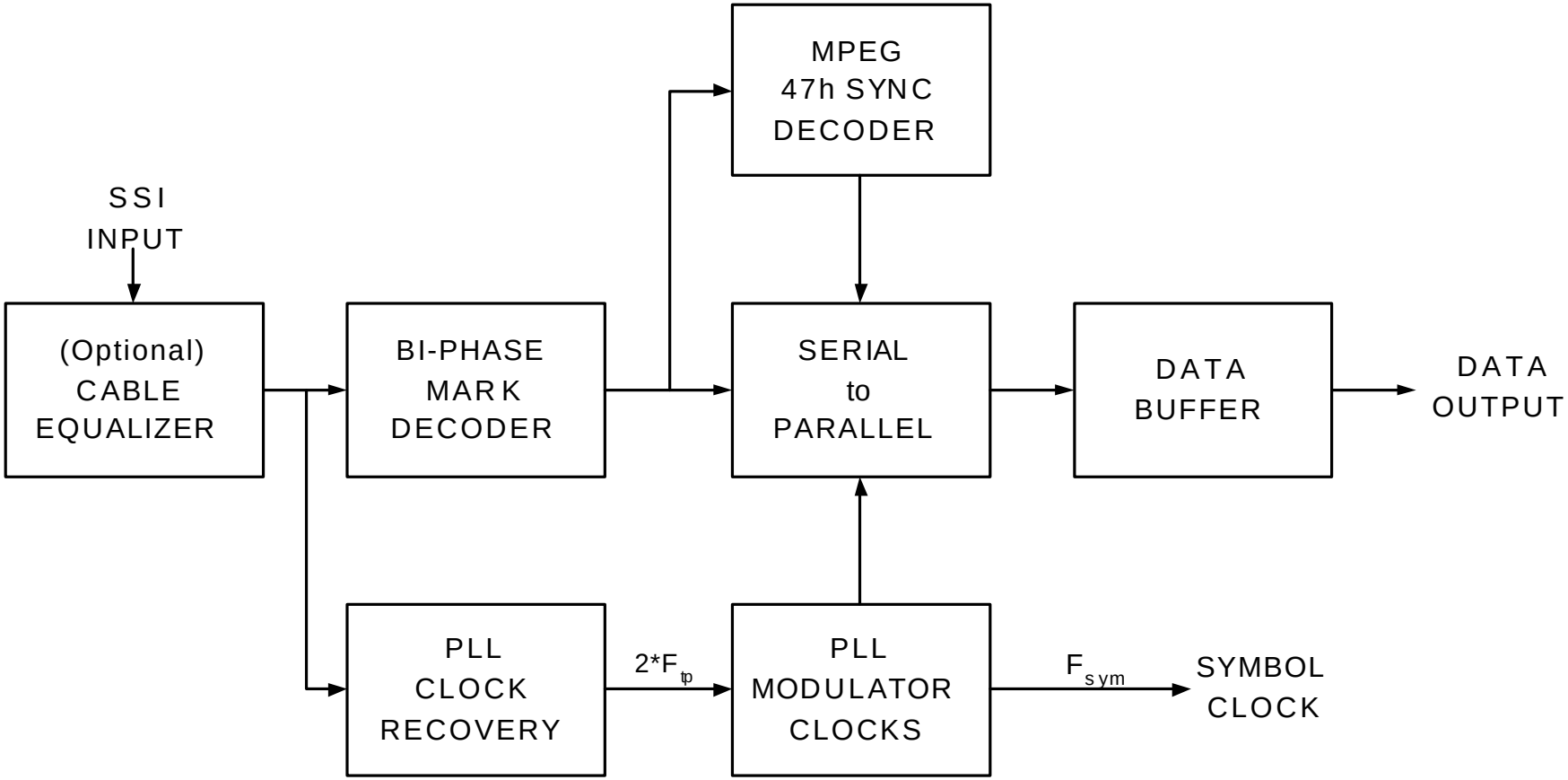
16-VSB: 38.78531692 Mbits/sec (N = 4)

Clock frequencies within ± 2.8 ppm (same as F_{sym})

SMPTE 310M TRANSMIT



SMPTE 310M RECEIVER



SMPTE 310M Clock Frequencies

Signal	Clock Frequency (MHz)	±2.8 ppm Drift (Hz)
Symbol Clock	10.762238	±30
8-VSB Transport Clock	19.392659	±54
8-VSB Interface Clock	38.785318	±108
16-VSB Transport Clock	38.785318	±108
16-VSB Interface Clock	77.570636	±216

$$F_{INT} = 2*F_{tp} = 2*N*(188/208)*(312/313)*F_{SYM}$$

N = 2 for 8T-VSB (2 data bits/symbol)

N = 4 for 16-VSB (4 data bits/symbol)

Symbol Clock Tests

- Measure SMPTE 310M signal *directly*
  - Clock frequency
    - Easy to measure with current test equipment (e.g. frequency counter)
    - Drift tolerance < 2.8 ppm; drift rate < 0.028 ppm/sec
  - Clock (edge) jitter (nsec, p-p)
    - Need good piece of test equipment to measure this (e.g. high speed scope or specialized unit)
    - Signal transitions < 2 nsec, p-p
- Measure SMPTE 310M signal *indirectly*
  - Transmission symbol clock phase sidebands
  - Reference receiver SNR @ white noise threshold

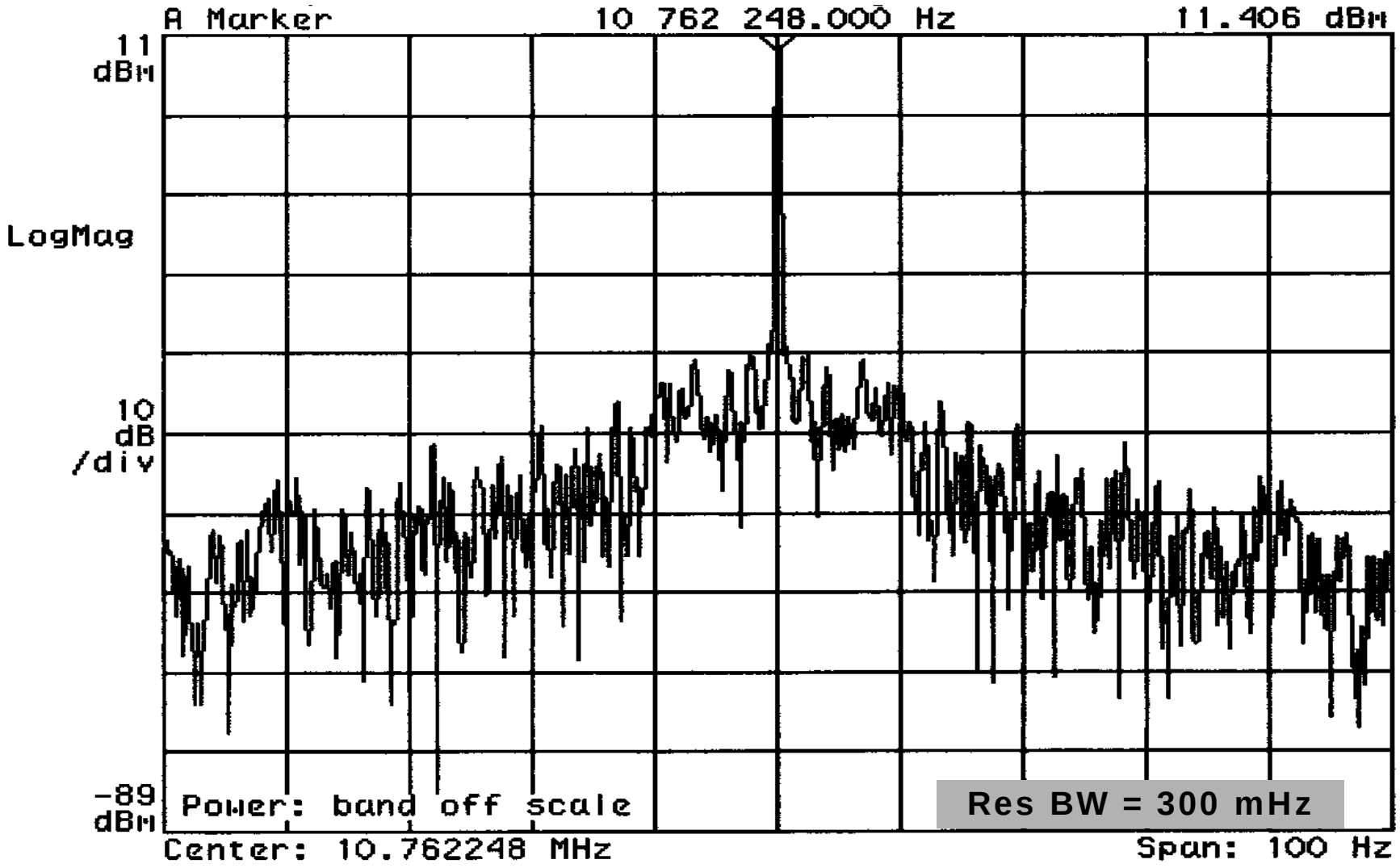
Current Difficulties

- Currently, SMPTE 310M clock issues have been observed in couple of cities doing DTV field testing
- Not a problem with standard, just implementation
- Two issues:
  - Clock *frequency* tolerance
  - Clock *jitter* tolerance
- Effect:
  - Reduction of effective white noise threshold in receivers
  - Bursty performance
  - *Not* noticeable on Agilent 89441 or RFA300 test equipment

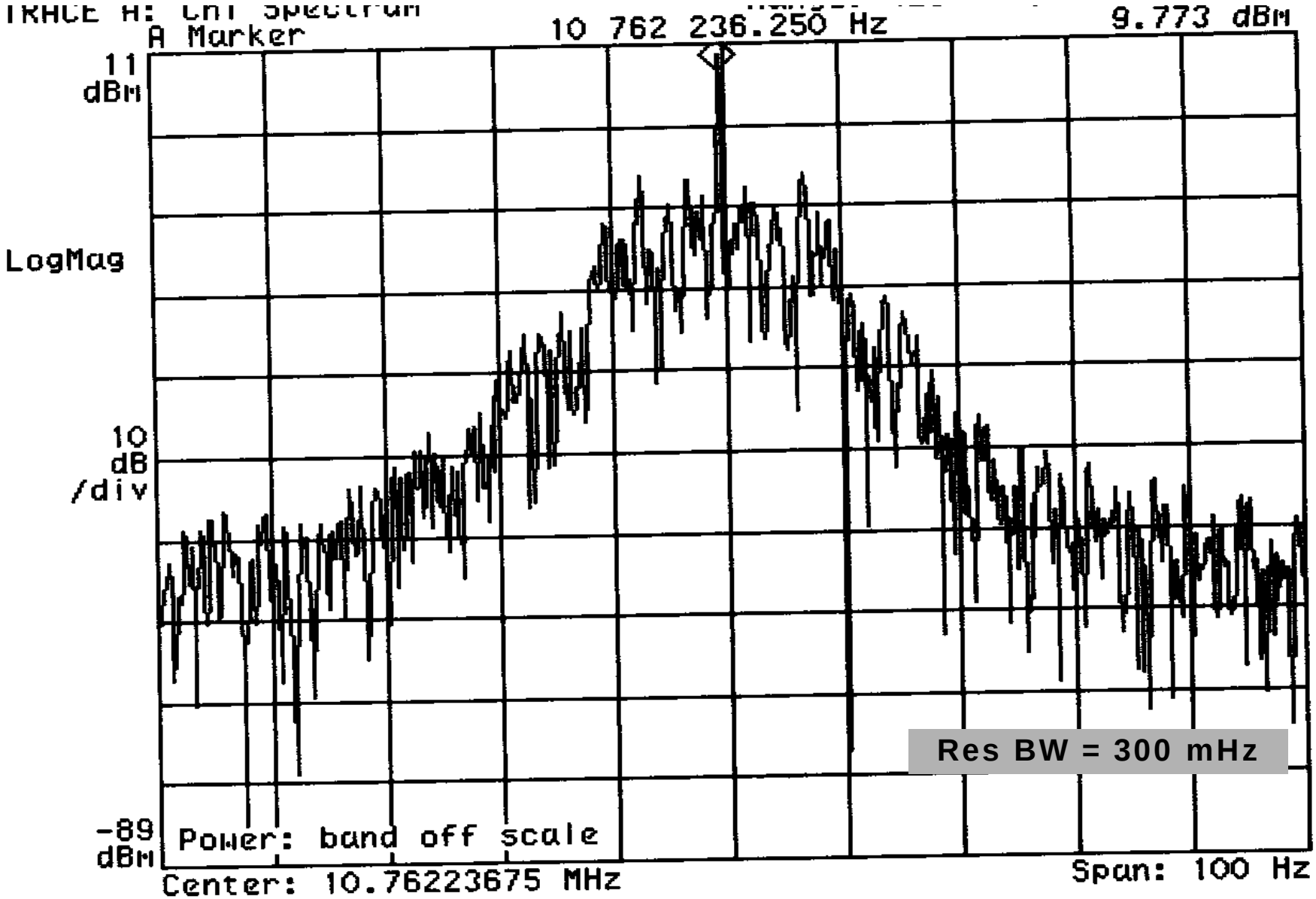
Symbol Clock Jitter

- Can creep into system anywhere
  - Transport (video) encoder
  - Any STL link (fiber, microwave)
  - SMPTE 310M interfaces
  - VSB modulator
- Symptoms: bursty errors at receiver
  - Moderate problem: near white noise threshold
  - Severe problem: even at strong signal levels
- Still looking for *convenient* way to measure jitter
- Currently only have *indirect* methods
  - Reference Rx white noise threshold degradation
  - Symbol clock modulation sidebands

Symbol Clock Spectrum - No Jitter



Symbol Clock Spectrum - With Jitter



SMPTE 310M Pluses

- Self Clocking
- Polarity Insensitive
- Low Component Count
- Relatively Inexpensive
- Bandwidth Efficient in RF Implementation

DVB ASI Pluses

- Mature Standard – Widely Implemented
- Robust Error Correction
- Includes Sync Byte
- Accepts a Variety of Bit Rates
- Electrically Identical to SDI (CCIR 601)

SMPTE 310M Minuses

- Uses NRZ Coding
- No Error Correction
- No Sync Bytes
- Jitter Sensitive
- Fixed Bit Rate once Implemented
- Limited Design and Field Experience

DVB ASI Minuses

- Polarity Sensitive
- Requires Wider Bandwidth in RF Implementations
- Higher Component Count
- Higher Cost to Implement

Practical Uses for DVB-ASI

- Decoder Output
- Intra-Facility Routing
- Localized Switching
- Input/Output of Storage Devices
- Input/Output of Bit Stream Manipulators
- Public Network Transport

Practical Uses for SMPTE 310M

- RF Transport
  - Over the air Broadcast
  - STL
  - RPU/ENG
- Efficient Bit Stream Storage

More Information

DVB/ASI – DVB Document A010

Interfaces for CATV/SMATV Headends and Similar Professional Equipment

SMPTE 310M-1998

Synchronous Serial Interface for MPEG-2 Digital Transport Stream

Acknowledgements

Gary Sgrignoli – Zenith Corporation

David Horowitz – Horowitz Television Technology

Jim Kutzner – Advanced Television Technology Center

Ed Williams – PBS DTV Strategic Services Group

Gregory Forbes – PBS Engineering

Rudy Pruitt – PBS Engineering Lab

Great Training Opportunity

ATSC
VSB Transmission System
Tutorials

Zenith – SBE – State Broadcast Associations
Private Companies

YOUR TURN

Questions?

Discussion?

Debate?